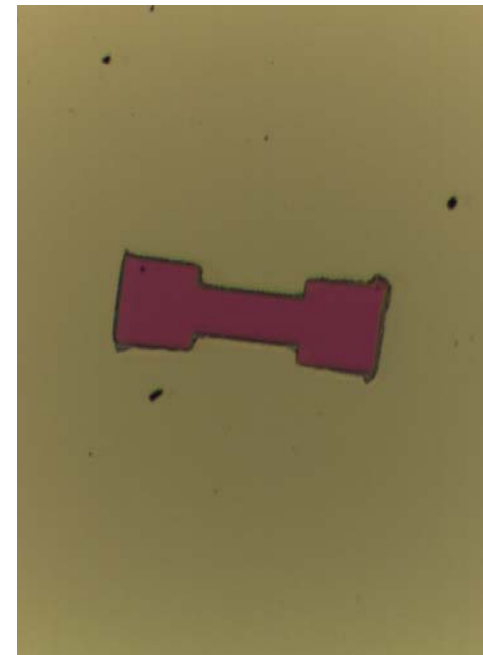

GRAPHENE FET DEVICE FABRICATION USING DIRECT WRITE LITHOGRAPHY

KATHY THACH, ALEX JACOBSON, LESTER LAMPERT, JUN JIAO



OVERVIEW

- I. Current Challenges with Computer Processors
- II. Graphene
 - I. Electronic quality
 - II. production
- III. FET Devices
- IV. Direct-Write Lithography
 - I. photolithography
- V. Summary and Acknowledgments



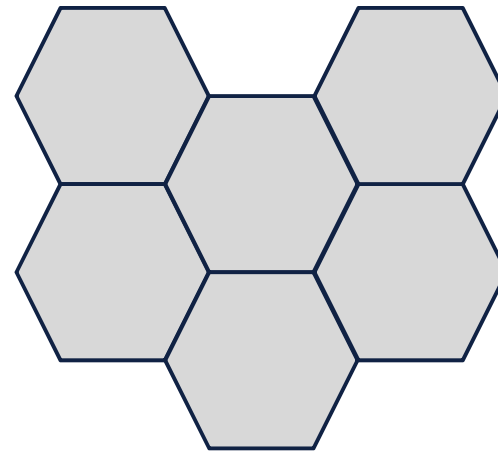
Device

MOORE'S LAW: A REAL LIMIT?

- Moore's Law: number of transistor in a processor will double every two years
- Problematic because current materials in transistors become unreliable if they are scaled down any further
- Nano-size copper interconnects lose conductance and overheats⁷
- Semiconductor companies require a new material that is reliable and conductive at the nano-scale, which can be used for transistors and interconnects

GRAPHENE

- 2-D honey-comb lattice carbon atoms²
- Zero-gap semiconductor
- Thin and strong, absorbs little light
- Can be cut down into true nm-size
- Popular because of its high electronic quality^{4, 1,6}



Hexagonal shape of graphene

ELECTRONIC QUALITY OF GRAPHENE

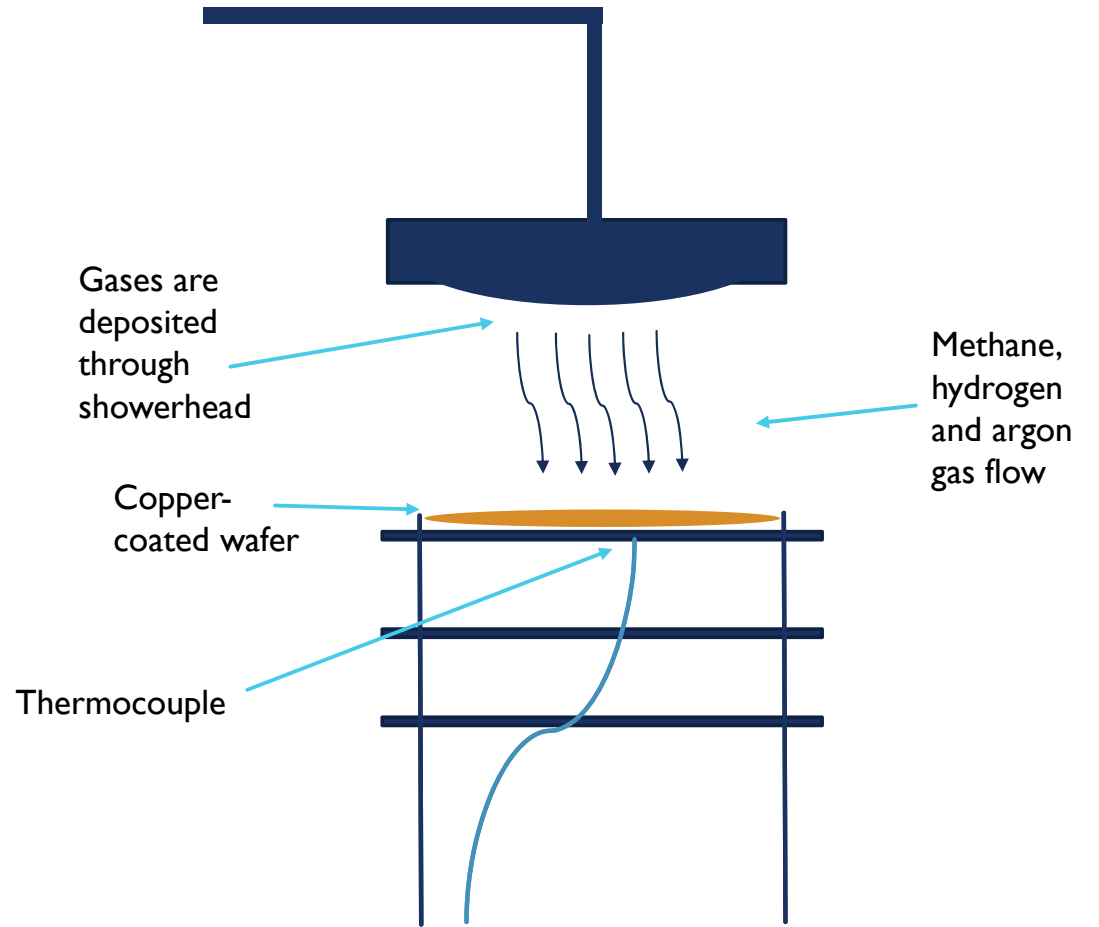
- Ballistic transport at submicron level
- High mean free path_{2,4}
- Immune to electro-migration
 - Electrons will not scatter when traveling on graphene

GRAPHENE GROWTH

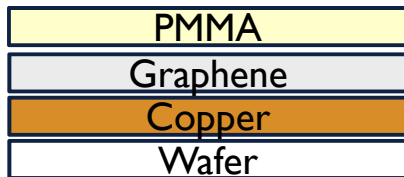
- Chemical Vapor Deposition
 - Copper catalyst: physical vapor deposition
 - Methane and hydrogen gas ratio
- Grown graphene is transferred to substrate using wet chemistry methods



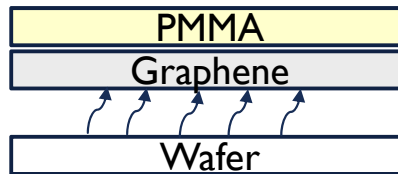
Cold Wall Furnace



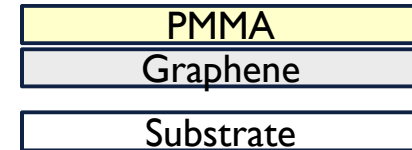
Graphene Transfer Process



PMMA coating:
PMMA is applied through
spin coating



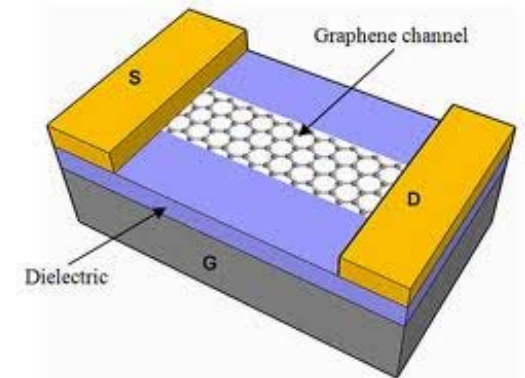
Copper etching using
 FeCl_3 :
PMMA is hydrophobic
and rises to top of
solution with graphene

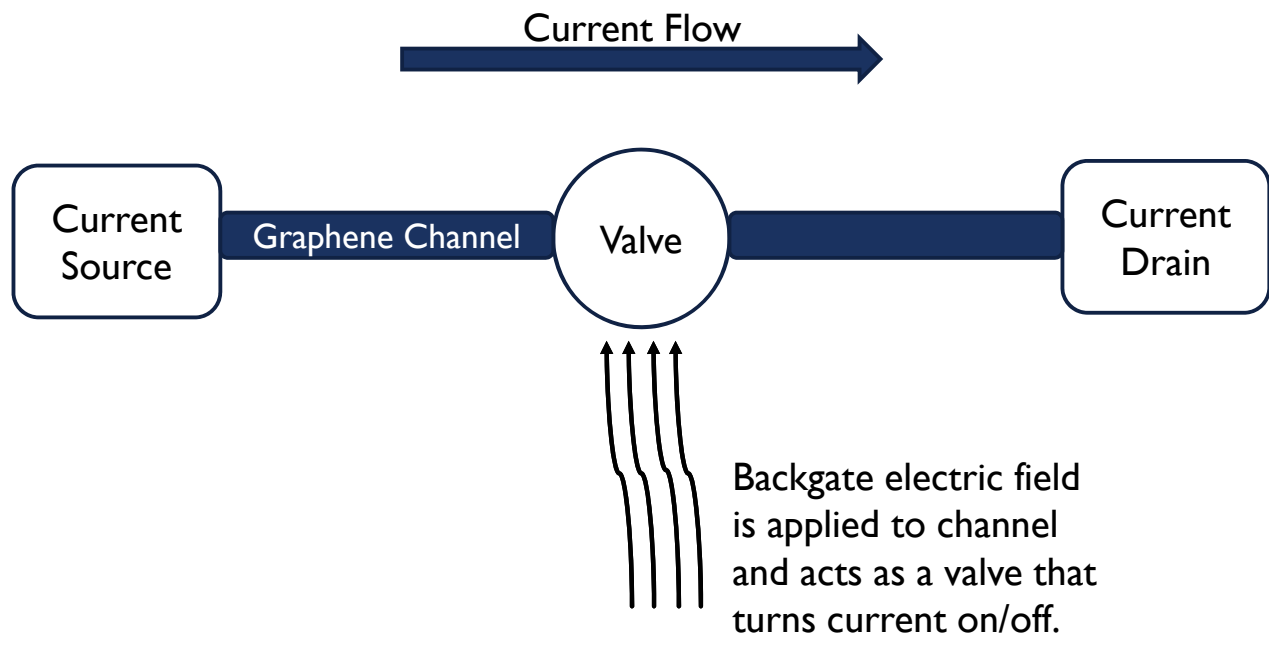


Graphene Transfer to
substrate

FET DEVICES

- Field Effect Transistors controls the flow of electrons from source to drain
- Can control conductivity of a semiconductor





DIRECT-WRITE LITHOGRAPHY

- DWL is done using a modulated laser that exposes a photoresist-coated silicon wafer
 - Negative SU-8 photoresist
- Pattern is created in Paint or Autocad and info is put into Lab View Program
- Basic Procedures: focus on sample, collect a sample plane, start patterning

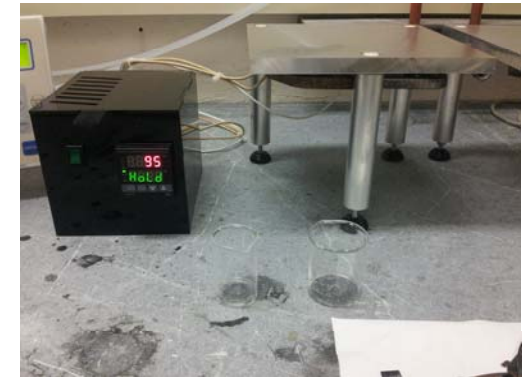
BASIC PROCEDURES



Silicon Wafer is coated with SU-8 and is soft-baked at 95 C



Laser exposure



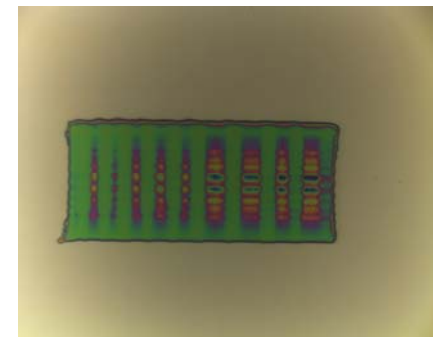
Post-exposure bake and development

TEST PATTERNING

- Settings
 - Velocity
 - Resolution
 - Modulator
 - Purpose of tests: determine the best settings for devices
- Tests done on wafer combining a variety of resolution and velocities



Res.: 5 microns
Vel.: 2 rpm



Res.: 1 microns
Vel.: 2 rpm

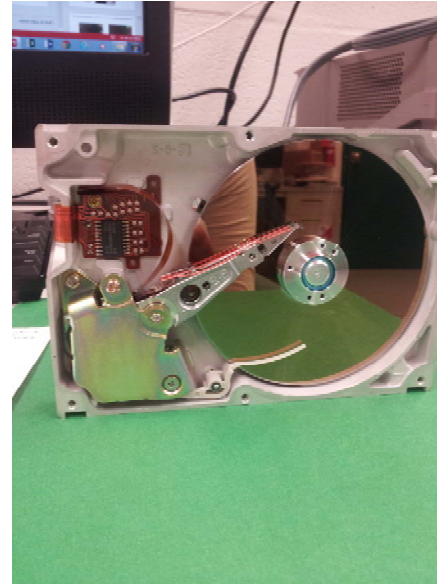
- Variety of tests were done to analyze the effects of each variable
- Trial 1 and 2 showed a smaller step size created better patter
- Trials 3 and 4 showed a lower velocity is best (.05-1 rpm)
- Trials 5 and 6 showed that a velocity closer to 0.50 works best, laser intensity primarily does not effect pattern
- Approximately 100 trials were using a combination of these settings

Trial #	Wafer #	Resolutions (um)	Velocities x & y (rpm)	Modulator Setting
1	1	20,10, 5, 1	0.05	1
2	2	20, 10, 5, 1	0.10	1
3	3	5, 1	7-10	1
4	4	5, 1	1-6	1
5	5	1	.05-1	3
6	6	1	.05-1	1

Test Patterning Matrix

HIGH SPEED LASER SHUTTER

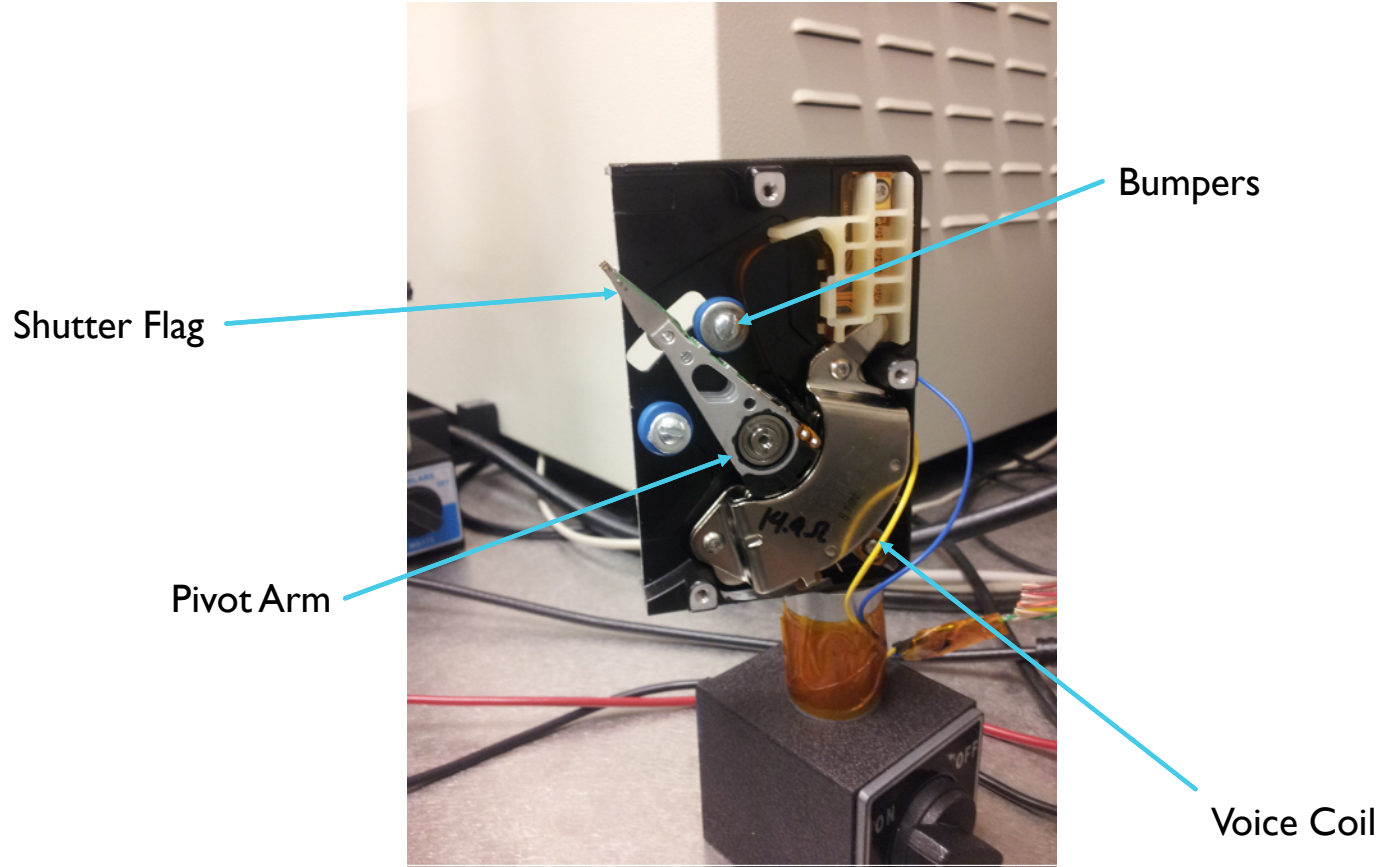
- Shutter is made from a recycled hard-drive
- Mechanics already available: voice coil controls pivot arm
- Controlling amount of current that goes through voice coil and limiting swing length is crucial for a long-lasting shutter



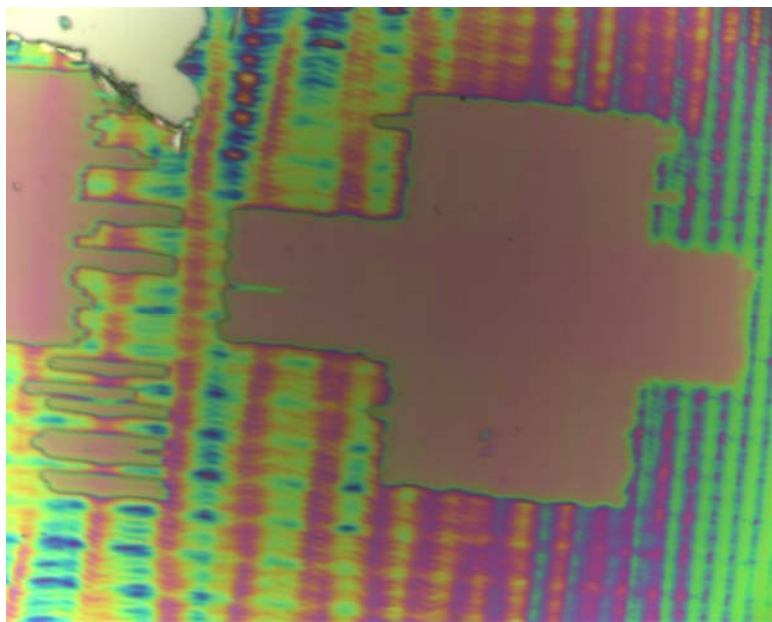
Hard Drive



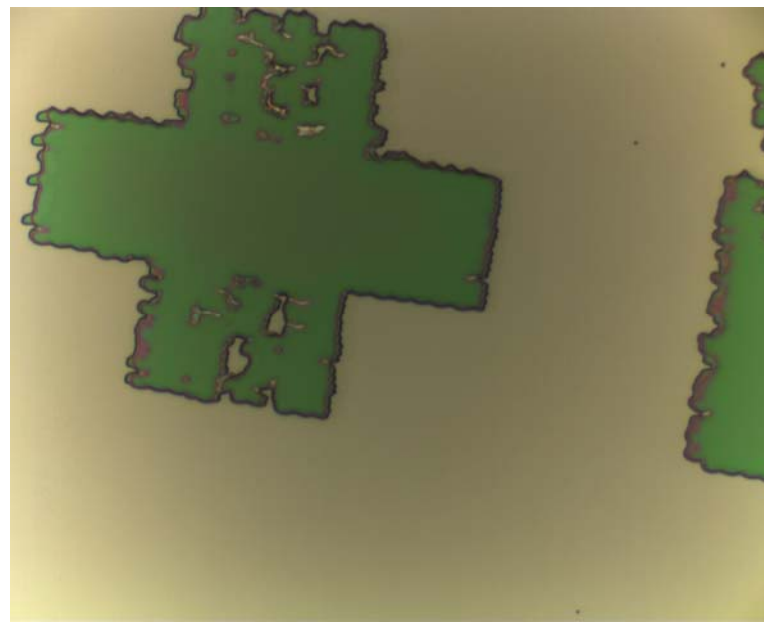
Laser shutter version 1



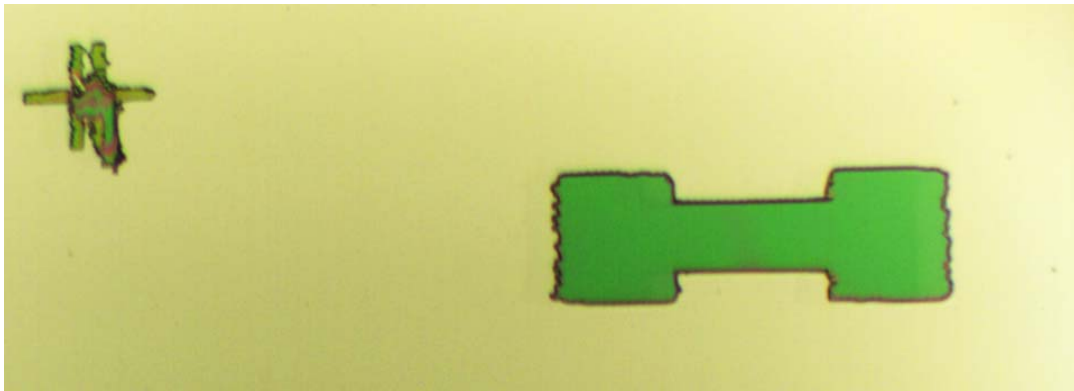
Laser Shutter Version 3



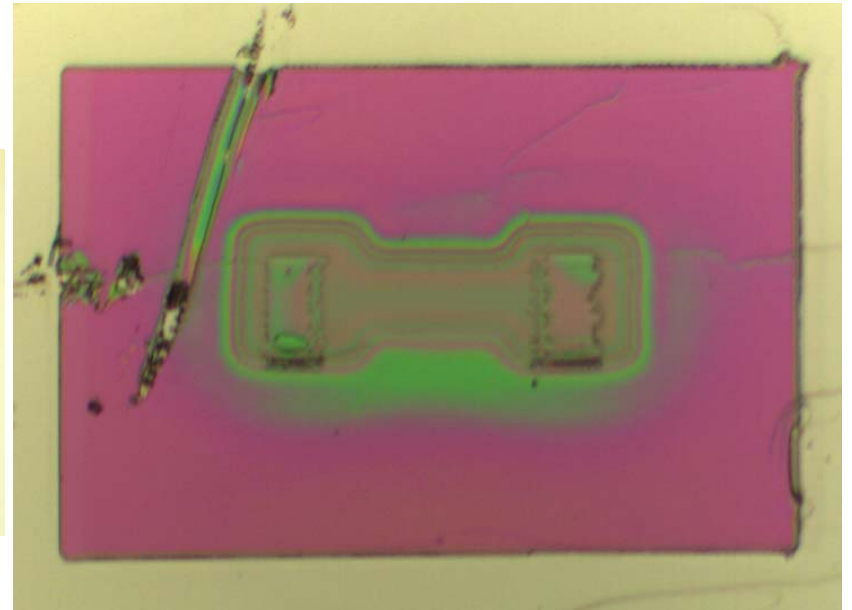
Pattern without laser shutter



Pattern with laser shutter



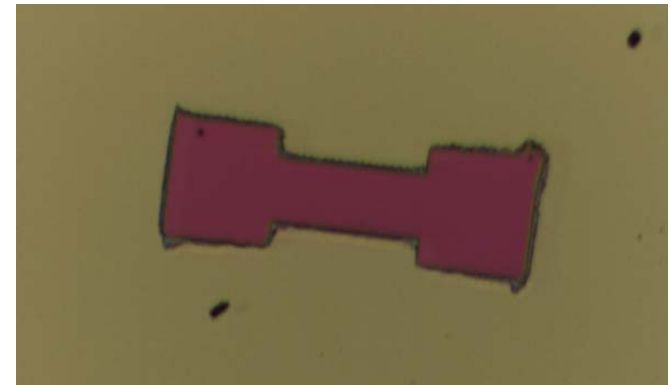
Stage 1



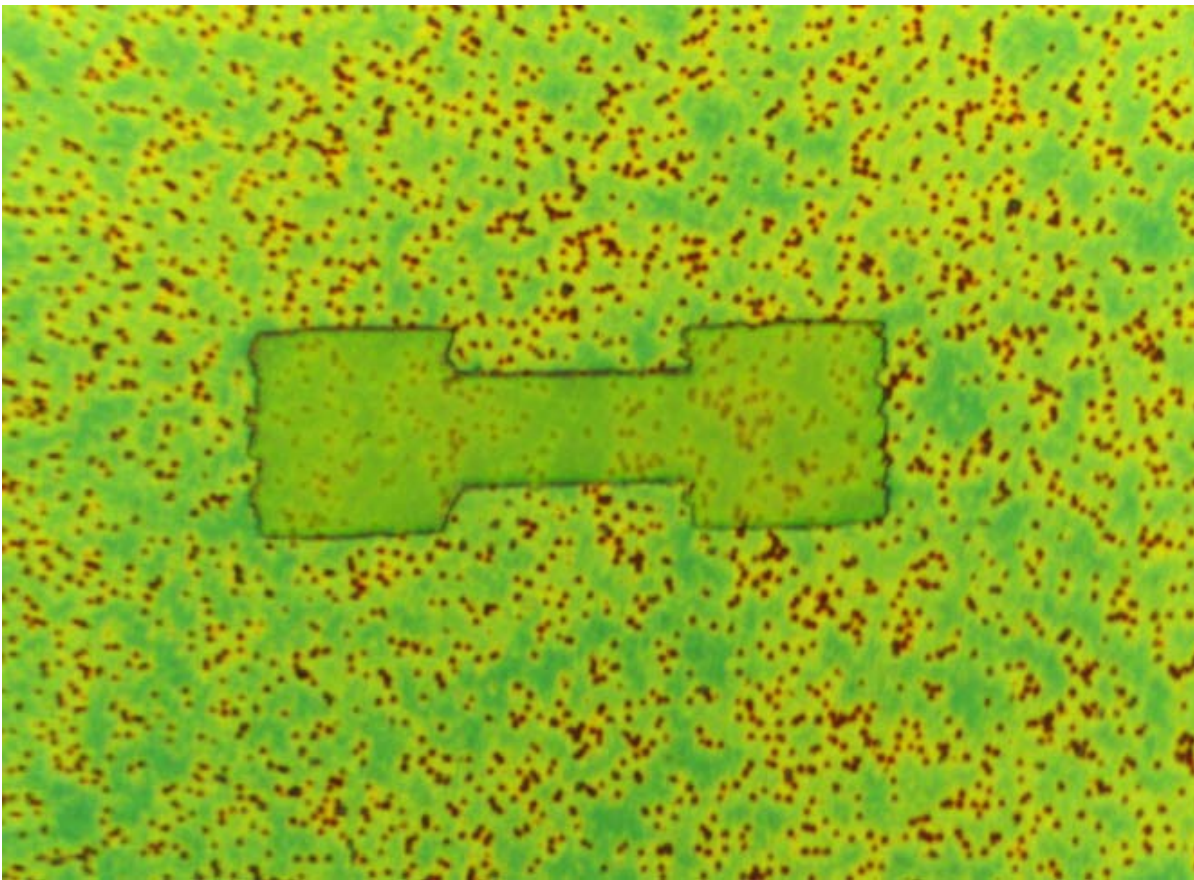
Stage 2

DEVICE FABRICATION

- Devices will be fabricated out of graphene
- Graphene will be coated with resist, patterned, then remaining graphene will be removed using Oxygen plasma



Device Mask



Graphene FET Device

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**Thank You for listening
Questions?**